J Mater Sci: Mater Electron (2022) 33:14627–14643

Transfer of graphene thin film obtained by PECVD method to *Au/p-Si* rectifier junction as interfacial layer and analysis of its barrier characteristics depending on sample temperature

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Received: 10 December 2021
Accepted: 4 May 2022
Published online: 28 May 2022

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ABSTRACT

It is well known that in metal–semiconductor rectifier junctions with an interface layer, the drop potential across the interface layer modifies the barrier height by changing the electric field in the semiconductor. Therefore, examining the barrier characteristics of such structures depending on the sample temperature is important in the development of novel devices. Based on this assumption, in order to interpret the barrier characteristics of the *Au/Graphene/p-Si/Al* structure in detail, its current–voltage (*I–V*) measurements were measured under dark conditions in the temperature range of 120–320 K in 20 K steps. Graphene thin film was grown on copper foil by plasma-enhanced chemical vapor deposition (PECVD) method and then transferred as an interfacial layer on the clean and polish surface of *p-Si* semiconductor base material made ohmic contact with aluminum metal. After examining the morphological and optical properties of the produced film, the gold metal was evaporated onto the film under vacuum conditions to have a circular contact area of 1 mm diameter, as it is necessary for electrical measurements. Various characteristic parameters such as ideality factor, barrier height, saturation current, threshold voltage, rectifying ratio, and series resistance of *Au/Graphene/p-Si/Al* structure were calculated from *I–V* measurements taken depending on sample temperature using Rhoderick, Norde, Cibils, and Chattopadhyay methods. The obtained results were interpreted comparatively on the basis of Tung's inhomogeneous barrier model.

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https://doi.org/10.1007/s10854-022-08382-8

1 Introduction

Metal–semiconductor junctions, which appear in the form of rectifier and non-rectifier (ohmic), are important components of any semiconductor device. These junctions still have great technological interest due to their versatile applications in different fields of modern electronics [1–6]. The shape and size of the potential barrier that occurs at the metal–semiconductor rectifier junction depends on the charge distribution in the space charge region in the semiconductor, the interface states, and the properties of the interfacial layer. While the interfacial layer at such junction often appears as an oxidized layer of the semiconductor material used, sometimes an interfacial layer can be also formed by placing a thin insulator layer with different properties between the metal and the semiconductor [2–4]. Thus, the metal–semiconductor junction turns into a metal–insulator–semiconductor junction, and the barrier characteristics of this junction are tightly dependent on many parameters such as the thickness, homogeneity, and morphological structure of the interface layer used. Since barrier parameters such as ideality factor, barrier height, saturation current, threshold voltage, rectification ratio, and series resistance are sensitively dependent on the interfacial layer, researchers working in this field continue to investigate the effects of interfacial layers with different properties obtained by different methods on metal–semiconductor rectifier junctions in order to develop alternative devices [7–24].

Due to its extraordinary properties and the diversity of its technological applications, graphene is still a very important material that attracts the attention of researchers today. Many techniques such as mechanical exfoliation [25], liquid-phase exfoliation of graphite [26], epitaxial growth [27] chemical reduction of graphene oxide [28], chemical vapor deposition (CVD) [29], and plasma-enhanced chemical vapor deposition (PECVD) [30, 31] are used in the production of graphene thin films. Among these, PECVD technique is the most widely used recognized technology for high quality, large area, and low temperature thin film deposition. The other advantages of PECVD technique are that it provides catalyst-free and transfer-free growth at a relatively low temperature. In the PECVD technique, which is based on the use of plasma produced at low pressure, free electrons accelerated by the electric field created by a bias voltage gain sufficient kinetic energy and collisions between these electrons and gas molecules cause excitation, ionization, and dissociation processes along with bonding. Various reactive species included in the glow discharge give the opportunity to process materials at temperatures lower than 400 °C. These species diffuse into the substrate, followed by highly complex surface reactions such as physical or chemical adsorption, desorption, surface reaction process, and surface ion bombardment for film formation [32].

As stated in the paragraphs above, since traps in metal–semiconductor devices, undesirable crystal structures and interface states cause various problems on device performance, it is very important to control the electrical behavior between metal and semiconductor by passivating these effects. Today, in order to reduce such problems, various metal oxides, insulators, and organic materials obtained by different techniques are placed in the form of thin films between metal and semiconductor in device production. In this study, to see the passivation effects of graphene, which is an excellent material, on the interface, graphene thin film deposited by PECVD technique was used as an interlayer to control its electrical properties by passivating the undesirable dangling bonds at the interface of the *Au/p-Si* rectifier junction. The electrical measurements of the *Au/Graphene/p-Si/Al* structure produced under laboratory conditions were taken depending on the sample temperature, and the junction parameters, which were sensitive to the structural and electrical properties of the interfacial layer, were investigated with different techniques. The results show that, in addition to various interlayers used in other studies [7–24], graphene interlayers deposited with the PECVD technique can be safely used in innovative device applications.

2 Experimental procedure

In the first stage of the experimental work, the graphene thin film to be used as the interfacial layer was obtained on the copper foil substrate in the PECVD device. After being chemically cleaned and dried, the copper foil substrates were placed in the vacuum chamber of the PECVD device. The pressure of the chamber of the device was reduced to 10^{-4} mTorr. Copper foils were annealed at 1000 °C using H_2/Ar

gas so that graphene could grow as a single layer on the substrate. Graphene films were grown using H_2, Ar, and CH_4 gases as the initiator monomers, at 600 °C for 30 min at 100 W radio frequency power. The flow rates of H_2, Ar, and CH_4 initiator monomers gases were determined as 10 standard cubic centimeters per minute (sccm), 20 sccm and 15 sccm, respectively. The properties of the graphene film deposited on copper foil were investigated using scanning electron microscopy (SEM), atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), and Raman spectroscopy techniques.

In the second stage of the experimental study, the *p-Si* semiconductor substrate with a (111) orientation with a resistivity of 1–10 Ω-cm and a thickness of 400 μm was cleaned by the chemical cleaning procedure [33]. Since it is necessary for electrical measurements, Al metal was evaporated at about 10^{-7} Torr vacuum on the matte surface of the chemically cleaned semiconductor, and then thermally annealed at 580 °C for 3 min in N_2 environment.

In the third stage of the experimental study, graphene thin films produced on copper foil under certain conditions in the PECVD device were transferred onto the polished and cleaned surface of the *p-Si* semiconductor with ohmic contact. Polymethyl methacrylate (PMMA) material was used in the transfer process of graphene. First, the graphene thin film obtained on the copper foil was coated with PMMA and baked at 150 °C for 3 min. Then the copper foil was etched with $FeCl_3$ aqueous solution. After washing the PMMA/graphene structure with deionized water, it was placed on a *p-Si* substrate with *Al* ohmic contacts and then PMMA was removed with the help of acetone. Finally, in order to make electrical measurements using a certain contact area, *Au* metal was evaporated onto the graphene thin layer at 10^{-7} Torr. Thus, the contact area was determined as 7.85×10^{-3} cm^2.

In the fourth stage of the experimental study, electrical measurements of the produced *Au/Graphene/p-Si/Al* structure were carried out in 20 K steps in the sample temperature range of 120–320 K under dark conditions. The HP model 4140B picoammeter with temperature-controlled Leybold Heraeus closed-cycle helium cryostat was used in the electrical measurements.

3 Results and discussion

The operational steps of transferring the graphene thin film deposited under certain conditions on copper foil in the PECVD device to the p-Si substrate with the help of PMMA are shown in Fig. 1a. Before starting the transfer processes, to reveal the morphological properties of the graphene thin film, SEM (Fig. 1b) and AFM (Fig. 1c) images were obtained. The granular graphene thin film is quite obvious from these images. In addition, it can be said that the graphene film has a smooth and uniform surface morphology, almost free of common morphological defects such as pinholes, cracks, traps, and voids. The chemical and electronic states of atoms in a material can be determined by the XPS technique. Analysis of the C–C bond of graphene by this technique is shown in Fig. 1d and the binding energy was determined to be approximately 284 eV. It is well known that Raman spectroscopy is one of the most important techniques used to investigate the structural and electronic properties of graphite materials. In addition, with this technique, information can be also obtained about the crystallization quality of graphene sheets. The Raman spectrum of the graphene thin film is presented in Fig. 1e. It appears from the figure that the G band of graphene corresponds to approximately 1560 cm^{-1} and the 2D band at 2700 cm^{-1}. While the G band shows the in-plane vibration of the sp^2 hybridizing carbon atoms, the 2D band is formed as a result of the second-order Raman scattering process. The D band, which consists of defects in sp^2 hybridizing carbon atoms and lattice distortions, is not observed. In addition, the quality of the deposited graphene was evaluated by calculating the ratio of the intensities of the 2D and G peaks (I_{2D}/I_G). This ratio is 1.11. Therefore, since the I_{2D}/I_G ratio is 1.11 and there is no D peak, it can be said that good-quality graphene was synthesized.

In order to reveal the current-conduction mechanism in the structure, it is very important to make electrical measurements in two- or three-terminal devices such as diodes and transistors, depending on the sample temperature. In this way, the character of the potential barrier where the rectifying process takes place can be revealed. In such analyses, it is important to examine the parameters such as ideality factor, barrier height, saturation current, threshold voltage, rectification ratio, interface state density, and series resistance as they reflect the character of the

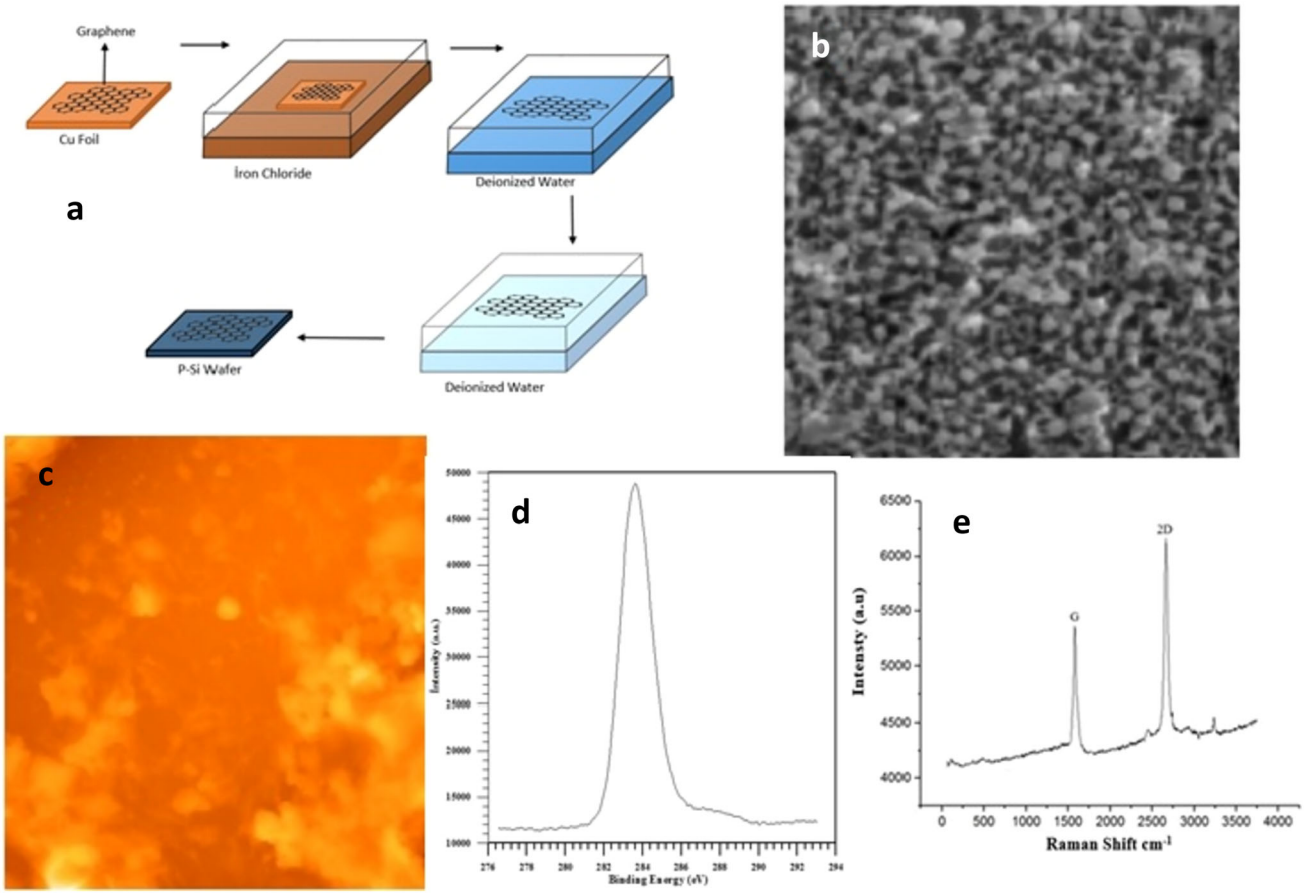


Fig. 1 **a** Transfer of graphene thin film deposited by PECVD method onto p-Si substrate, **b** SEM image, **c** 2D AFM image, **d** XPS spectrum, and **e** Raman spectrum

barrier. In the study, these parameters were investigated in detail with conventional thermionic emission (Rhoderick method), modified Norde, Chattopadhyay, and Cibils methods.

The calculation of the parameters started by drawing the forward bias current–voltage–temperature (*I–V–T*) plots of the *Au/Graphene/p-Si/Al* structure is given in Fig. 2. The threshold voltage values, which are defined as the forward bias voltage at which the diode starts to conduct fully [34], were determined from the points where the lines fitted to the linear parts of the graphs intersect the voltage axis depending on the sample temperature. At the same time, the specific on-resistance (R_{on}) values were determined at each sample temperature by using the slopes of the linear fits made on these plots [35]. It is seen in the graph in the inset of Fig. 2 that the threshold voltage and R_{on} values are tightly dependent on the sample temperature. Both parameters have been decreased rapidly with increasing sample temperature. That is, the voltage required to produce a given current decreases with increasing temperature, and it can be said that this is caused by the temperature dependence of the carrier concentration, the energy bandgap, and the effective density of the states [36]. Also, Table 1 shows that the threshold voltage values changed from 411 mV at 320 K to 900 mV at 120 K and R_{on} values changed from 2.8 kΩ at 320 K to 24 kΩ at 120 K. Thermal decay coefficient (K_j) for junction was obtained as – 2.41 mV/K from a numerical fit using both the threshold voltage–temperature plot in the inset of Fig. 2 and the equation $K_j = -\Delta V_{threshold}/\Delta T$. Again, threshold voltage—R_{on} relationship is presented in the inset of Fig. 2. R_{on} values increased with increasing threshold voltage values depending on the decreasing sample temperature. The increase in threshold voltage and R_{on} values with decreasing sample temperature can be attributed to the fact that the free carrier concentration in the semiconductor is directly related to the

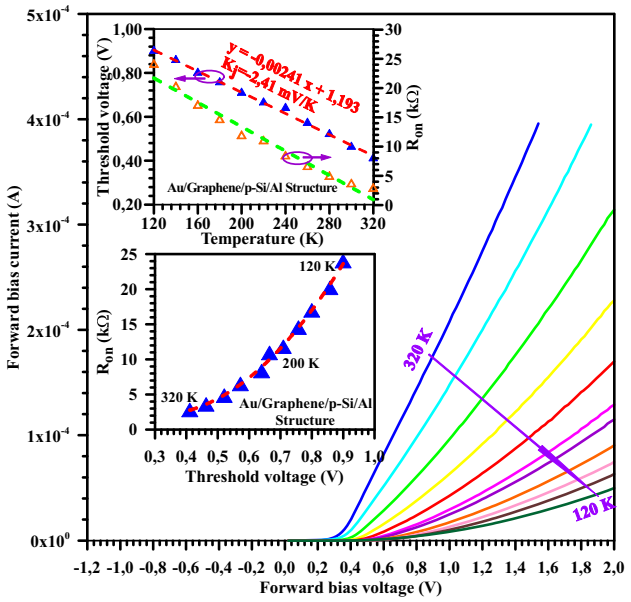


Fig. 2 The forward bias *I-V* characteristics of the *Au/Graphene/p-Si/Al* structure in the low temperature range of 120–320 K. Threshold voltage—R_{on}—temperature and threshold voltage—R_{on} plots are shown in the inset of graph

decrease with temperature. At the same time, the threshold voltage can be also defined as the forward bias voltage where there is no band bending in the semiconductor, that is, the bands are in the flat band state. Since the electrical field at the junction is zero, the diode becomes fully conductive in this case. However, since the concentration of free carriers in the semiconductor is temperature dependent, with increasing sample temperature, many free carriers may pass through the junction before reaching the flat band state, causing a large current to be produced and thus lowering the threshold voltage.

The dominant current mechanism in metal–semiconductor rectifier junctions produced from moderately doped semiconductors is thermionic emission. According to this theory, only charge carriers with energy greater than the potential barrier can cross over the barrier and create junction current. The relationship between current and voltage in such a junction is expressed by the following equation for the forward and reverse bias regions [1–4];

$$I = I_o\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

In this relation, I_o is the reverse bias saturation current given by the following equation;

Table 1 Parameter values obtained using different methods from forward bias *I–V* characteristics of *Au/Graphene/p-Si/Al* structure as a function of sample temperature

Sample temperature →		320 K	300 K	280 K	260 K	240 K	220 K	200 K	180 K	160 K	140 K	120 K
I–V method	n	1.706	2.035	2.229	2.552	2.897	3.175	3.443	3.814	4.193	4.580	4.805
	I_0 (A)	3.22×10^{-9}	2.91×10^{-9}	1.35×10^{-9}	4.49×10^{-10}	1.40×10^{-10}	5.14×10^{-11}	1.99×10^{-11}	4.62×10^{-12}	3.26×10^{-12}	8.69×10^{-13}	8.75×10^{-14}
	Φ_b (eV)	0.820	0.768	0.732	0.701	0.668	0.628	0.584	0.545	0.486	0.438	0.396
	Φ_{bF} (eV)	1.264	1.377	1.425	1.547	1.662	1.707	1.718	1.775	1.732	1.706	1.629
	Threshold voltage (V)	0.411	0.463	0.521	0.572	0.640	0.665	0.709	0.757	0.800	0.858	0.900
	R_{on} (kΩ)	2.80	3.59	4.85	6.52	8.34	10.92	11.81	14.54	16.98	20.19	24.00
Norde method	Φ_b (eV)	0.788	0.747	0.728	0.683	0.638	0.606	0.548	0.504	0.490	0.397	0.336
	R_s (kΩ)	0.16	0.16	0.22	0.28	0.34	0.43	0.53	0.60	0.68	0.76	0.84
Chattopadhyay method	n	1.967	2.151	2.250	2.400	2.501	2.571	2.653	2.732	2.820	2.910	3.036
	Φ_b (eV)	0.574	0.542	0.512	0.478	0.465	0.432	0.405	0.392	0.365	0.344	0.326
Cibils method	n	1.72	1.94	2.23	2.55	2.84	3.18	3.42	3.81	4.26	4.69	4.93
	R_s (kΩ)	1.82	1.86	1.93	1.97	2.05	2.13	2.23	2.31	2.40	2.48	2.57

$$I_0 = AA^*T^2\exp\left(\frac{-q\Phi_b}{kT}\right) \quad (2)$$

Other parameters in Eqs. 1 and 2 are defined as q electronic charge, V is bias voltage applied to the junction, n is ideality factor, k is Boltzmann constant, T is absolute temperature, A is junction active area (7.85×10^{-3} cm^2), A^* is Richardson constant (32 $Acm^{-2}\,K^{-2}$ for p-Si), and is Φ_b potential barrier height of junction, respectively.

The ideality factor characterizes the deviation of the I–V characteristics from the ideal (from the thermionic emission model) at the metal–semiconductor rectifier junction and can be written using Eq. 1 as follows:

$$n = \frac{q}{kT}\left(\frac{dV}{dlnI}\right) \quad (3)$$

Since only thermionic emission current will be involved in an ideal metal–semiconductor rectifier junction, the ideality factor is 1. However, factors such as tunneling, generation-recombination, image force effect, and biasing dependence of the barrier height may cause to deviate from the ideal state of I–V relationship in the junction. In the presence of these factors, n can be greater than 1.

In order to contribute to the realization of technological developments, the electrical performance of the fabricated metal–semiconductor rectifier junctions can be measured by physical parameters such as effective barrier height, ideality factor, series resistance, and threshold voltage. Common methods such as Rhoderick, Norde, Chattopadhyay, and Cibils methods can be used to obtain these parameters from the forward bias I–V characteristics. All of these methods are based on the thermionic emission model, whose I–V relationship is given by Eq. 1. Therefore, the parameters mentioned in this study were first calculated by the Rhoderick (I–V method) method and then by the Norde, Chattopadhyay, and Cibils methods. The forward and reverse bias ln(I)–V characteristics in the temperature range of 120–320 K of the *Au/Graphene/p-Si/Al* structure are shown in the Fig. 3. While there is a linear variation at low forward bias voltages at each temperature, downward bending is exhibited due to the effect of series resistance, interface layer, and interface states at large forward bias voltages [37]. In the reverse bias portion of the characteristic, the reverse bias current saturation was

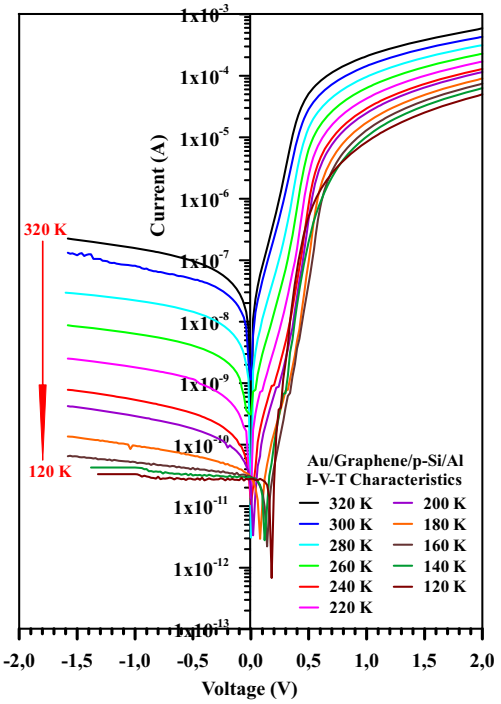


Fig. 3 The forward and reverse bias ln(I)–V characteristics of *Au/Graphene/p-Si/Al* structure in the temperature range of 120–320 K

observed when the reverse bias voltage increased at each temperature. I_o values were determined by using the points where the linear fit made to the forward bias part of the plots in Fig. 3 intersect the vertical axis at $V = 0$ and these values are presented in Table 1. At the same time, the variation of I_o values depending on the sample temperature is given in Fig. 4. It can be seen from this figure that the saturation current increases rapidly with increasing sample temperature. The change in saturation current in the temperature range of 120–220 K is given in the inset of this graph. The increase in I_o values with increasing sample temperature may be related to the temperature dependence of the threshold voltage [21].

It was observed that with decreasing sample temperature, the forward bias ln(I)–V curves shifted to the right. This shift indicates that larger forward bias voltage is required to achieve the same current value. As a result, the linear regions where the ideality factor and saturation current values were calculated also shifted to the right. The most important reason for this change may be the decrease in the energies of

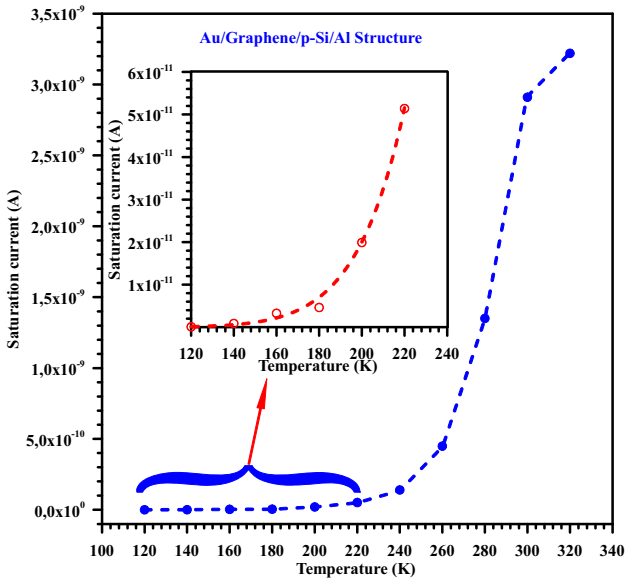


Fig. 4 Variations of leakage current with sample temperature for *Au/Graphene/p-Si/Al* structure. The variation of I_o–T in the range of 120–220 K is presented on the inset of the graph

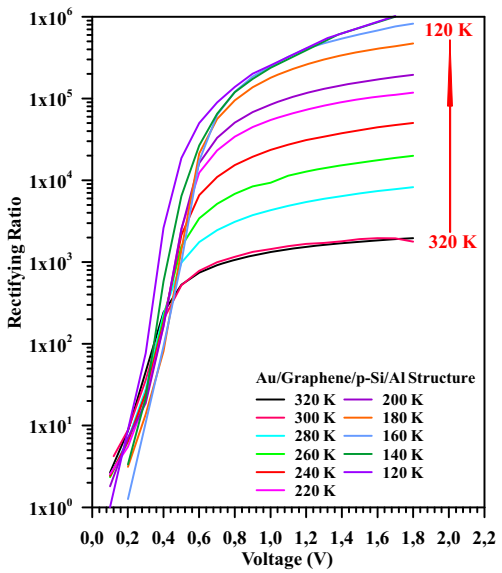


Fig. 5 Rectification ratio versus voltage changes as a function of sample temperature for the *Au/Graphene/p-Si/Al* structure

the free carriers with the decreasing sample temperature.

The asymmetric and non-linear *I–V* characteristics indicate that the *Au/Graphene/p-Si/Al* device has a rectifying character. In the ln(*I*)–*V* graphs in Fig. 3, the rectification ratios of the *Au/Graphene/p-Si/Al* structure were calculated from the ratio of the forward current to the reverse current corresponding to

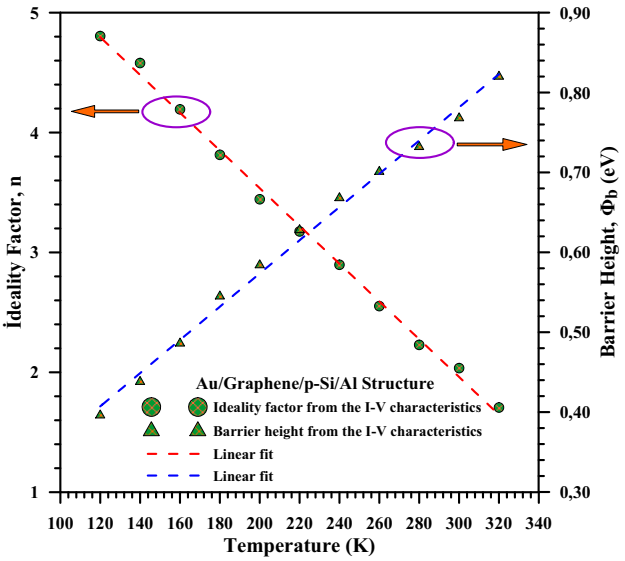


Fig. 6 The variations of n and Φ_b values depending on sample temperature for *Au/Graphene/p-Si/Al* structure

the same voltage values, depending on the sample temperature, and are shown in the Fig. 5. These plots show that the diode has good rectification performance (about 10^3). The interface properties of metal–semiconductor rectifier junctions have an important role on the electrical characteristics of the junction. The rectifying behavior is basically caused by potential barrier in the junction. An interfacial layer is introduced into the junction to improve the electrical properties. Such a layer helps control the redistribution of interface states or reduces chemical interaction at the surface [38].

The ideality factor values determined from the slopes of the linear regions of the forward bias ln(*I*)–*V* characteristics with the help of Eq. 3 are given in Table 1. The n value increased from 1.706 at 320 K to 4.805 at 120 K. The fact that the calculated n value at room temperature is greater than 1 indicates that the *Au/Graphene/p-Si/Al* structure is not ideal, and the interfacial layer, interface states, image force effect, series resistance, and inhomogeneous potential barrier are among the reasons for this situation [39–42]. At the same time, using Eq. 2 (arranging according to Φ_b in the form of $\Phi_b = (kT/q)\ln(AA^*T^2/I_o)$, the potential barrier height of the junction is calculated depending on the sample temperature and presented in Table 1. The Φ_b values decreased from 0.820 eV at 320 K to 0.396 eV at 120 K. Therefore, both n and Φ_b values are very strongly dependent on temperature. This situation is evident in Fig. 6. Figure 6 shows that

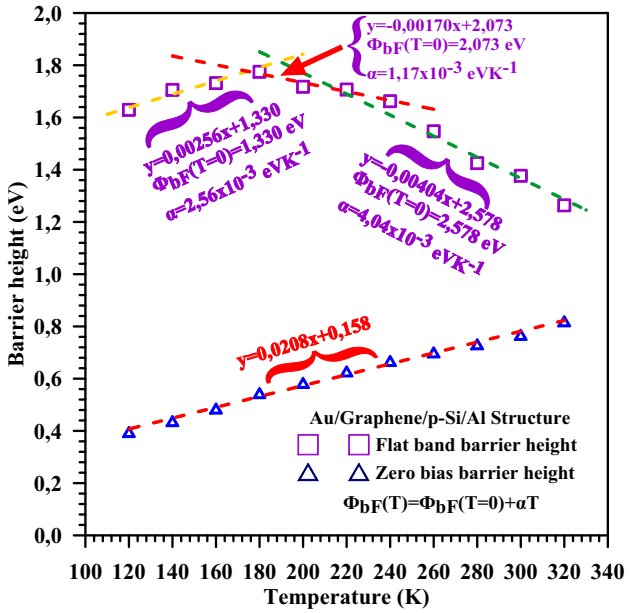


Fig. 7 Zero bias barrier height (Φ_b) and flat band barrier height (Φ_{bF}) as a function of sample temperature

n values decrease and Φ_b values increase with increasing sample temperature. Such dependence of n and Φ_b on sample temperature may be related to the inhomogeneity of the potential barrier. That is, there are potential barriers of different heights at the junction, and at low temperatures, electrons pass through low barriers, while at high temperatures they pass through high barriers [43]. As a result, it can be said that the potential barrier increases with increasing sample temperature. In general, the barrier height values in the devices can vary depending on many parameters such as the work functions of the contact materials and the properties of the constructed interface. A significant increase in the ideality factor and a decrease in the potential barrier height at low temperatures can also be caused by other factors such as thickness inhomogeneities and non-uniformity of interfacial charges [44].

Another important and fundamental parameter for the junction is the flat band barrier height (Φ_{bF}), which is measured in the zero electric field in the semiconductor unlike in the case of zero bias barrier height. Therefore, the effects of lateral inhomogeneities are not found on this parameter. Φ_{bF} parameter can be calculated from the Eq. 4 given below using the n and Φ_b values obtained from the experimental ln(I)–V characteristics:

$$\Phi_{bF} = n\Phi_b - (n-1)\frac{kT}{q}\ln\left(\frac{N_v}{N_a}\right) \quad (4)$$

where N_v is the effective density of states in the valence band of the *p-Si* semiconductor ($N_v = 1.04 \times 10^{19}(T/300)^{3/2}$ cm^{-3}) and N_a is the concentration of acceptor atoms ($N_a \approx 1 \times 10^{16}$ cm^{-3}). Also, the dependence of Φ_{bF} on temperature can be expressed as [45];

$$\Phi_{bF}(T) = \Phi_{bF}(T=0) + \alpha T \quad (5)$$

where α is the temperature coefficient. Variations of Φ_b and Φ_{bF} values depending on sample temperature are given in Fig. 7 and Table 1. It is seen in Fig. 7 that the zero bias barrier height increases with increasing sample temperature, while the flat band barrier height increases slightly in the range of 120–180 K, decreases slightly in the range of 180–240 K, and decreases more rapidly in the range of 240–320 K. According to Eq. 5, linear fitting of Φ_{bF} data provides 1.330 eV and 2.56 $\times$ 10^{-3} eVK^{-1} values in the range of 120–180 K, 2.073 eV, and 1.17 $\times$ 10^{-3} eVK^{-1} in the range of 180–240 K and 2.578 eV and 4.04 $\times$ 10^{-3} eVK^{-1} values in the range of 240–320 K for Φ_{bF} (T = 0) and α, respectively. It is seen that Φ_{bF} is larger than Φ_b in the whole temperature range of 120–320 K and this behavior is in accordance with the results in the literature [45–47]. Since the flat band barrier height is derived from the zero curvature of the conduction and valence bands, the I–V characteristic of the junction under these conditions is not affected by factors such as tunneling and image force lowering. In other words, the effects of lateral inhomogeneities on the potential barrier are eliminated.

To confirm Tung's suggestion pinch-off model [48], the linear relationship between the ideality factors and the zero bias barrier heights calculated at all measurement temperatures is presented in Fig. 8. The linear relationship between these two parameters is proof that the potential barrier is not homogeneous. That is, this situation can be explained by the lateral inhomogeneities of the barrier. From this graph, the lateral homogeneous barrier height for *Au/Graphene/p-Si/Al* structure was calculated as 0.908 eV from extrapolation of the barrier height at n = 1. According to Tung's model, there is a spatial distribution of patches of different heights in the junction, and this formation causes to deviate from the ideal state of the I–V characteristics.

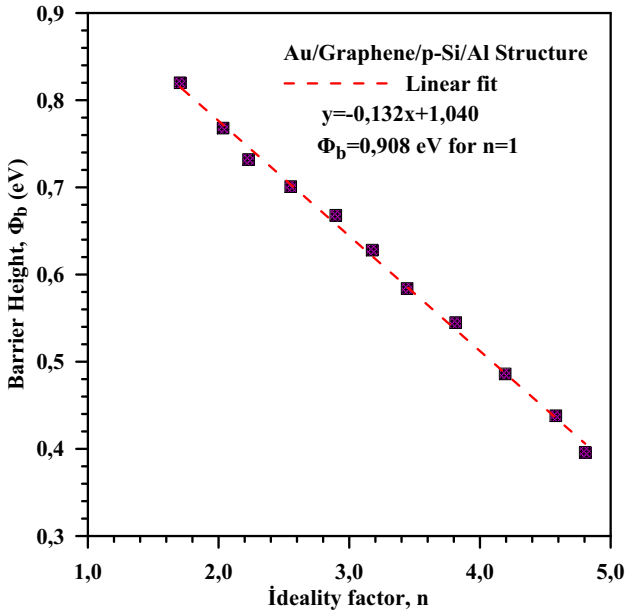


Fig. 8 Linear variation of zero bias barrier height versus ideality factor in the temperature range of 120–320 K for the *Au/Graphene/p-Si/Al* structure

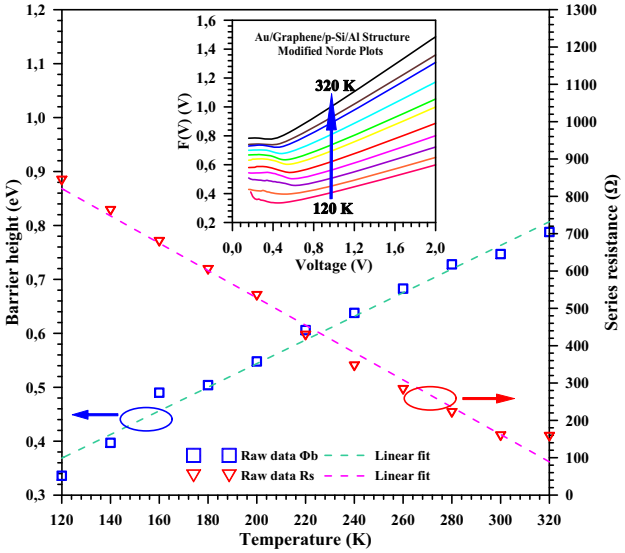


Fig. 9 The variation of the potential barrier height and series resistance values obtained from the modified Norde method depending on the sample temperature. The $F(V)$–V plots are also shown inset of this figure

Since parameters such as ideality factor, potential barrier height, and series resistance are important for rectifier junctions, different methods have been developed to calculate these parameters from experimental data [49–52]. Using the Norde method generalized by Bohlin, the barrier height and series resistance of the *Au/Graphene/p-Si/Al* structure were calculated by utilizing the forward bias I–V characteristics. Considering the current and voltage values corresponding to the minimum point of the $F(V)$ function $\{F(V) = (V/\gamma) - (kT/q)\ln[I(V)/AA^*T^2]\}$ defined in this method, potential barrier height $\{\Phi_b = F_m + [(\gamma - n)/n][(V_m/n) - (kT/q)]\}$, and series resistance $\{R_s = (\gamma - n)(kT/qI_m)\}$values are calculated as a function of temperature and the results are presented in Table 1 [50]. Quantities in the equations are described in reference 50. γ is an arbitrary constant greater than n. Variations of the Φ_b and R_s values calculated using this method depending on the sample temperature are shown in Fig. 9 and the $F(V)$–V plots are also shown inset of this figure. It can be seen from Fig. 9 that with increasing sample temperature, the series resistance decreases and the barrier height increases. That is, both parameters are strongly dependent on temperature. The variation of the device's series resistance with temperature can be associated with decreases in free carrier concentration at low temperatures [3, 4]. Since some of the applied bias voltage drops across the series resistance and this parameter is more effective at higher voltages, series resistance is one of the reasons why the forward bias ln(I)–V characteristics bend downward at sufficiently higher voltages. The reasons for the strong temperature dependence of the barrier height are the same as explained earlier in the text.

In addition, the ideality factor and barrier height values of the *Au/Graphene/p-Si/Al* structure can also be determined by the Chattopadhyay model. In this model, barrier height, surface potential, and inverse of ideality factor are expressed as follows, respectively [51];

$$\Phi_b = \Psi_s(I_c, V_c) + c_2 V_c + \frac{kT}{q} ln\left(\frac{N_v}{N_a}\right) \tag{6}$$

$$\Psi_s = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I}\right) - \frac{kT}{q}\ln\left(\frac{N_v}{N_a}\right) \tag{7}$$

and

$$c_2 = \frac{1}{n} = -\left(\frac{d\Psi_s}{dV}\right)_{I_c,V_c} \tag{8}$$

where $\Psi_s(I_c,V_c)$ is the surface potential corresponding to the critical current (I_c) and critical voltage (V_c) values. The N_v and N_a values used in Eqs. 6, 7 and 8 are the same as those given in Eq. 4 on page 8.

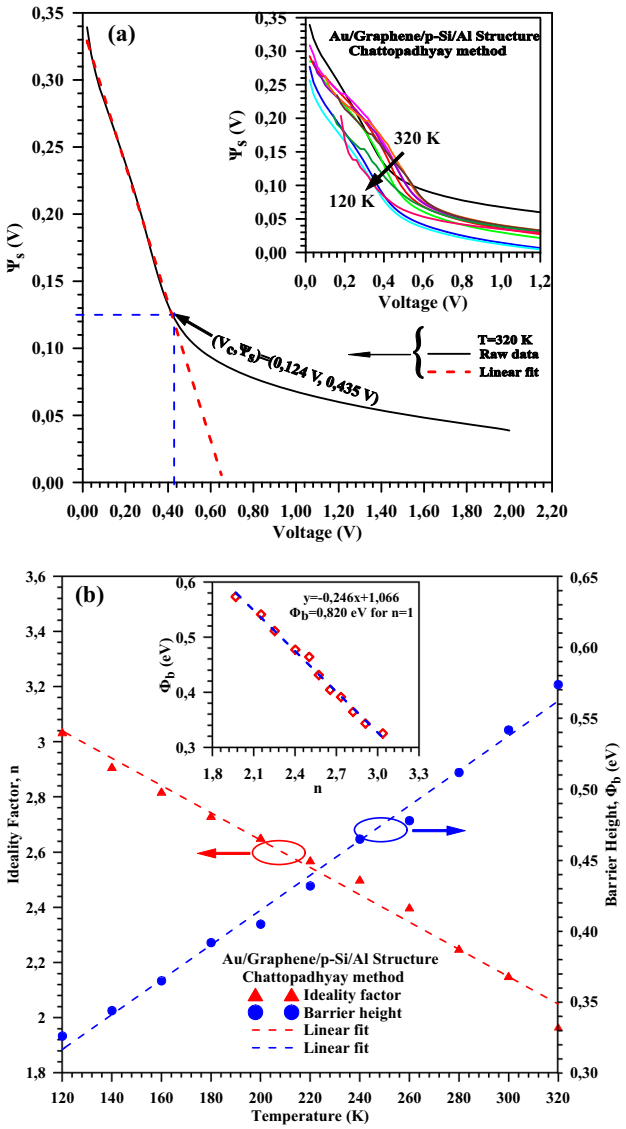


Fig. 10 **a** According to Chattopadhyay model, surface potential (Ψ_s) -forward bias voltage (V) plot for the *Au/Graphene/p-Si/Al* structure at T = 320 K. The Ψ_s–V changes in the 120–320 K range are shown in the inset of this figure. **b** Variations of n and Φ_b obtained from the Chattopadhyay model depending on sample temperature. The linear relationship between n and Φ_b is shown in the inset of this figure

Critical values indicate the point where the $\Psi_s - V$ plot starts to deviate from linearity. For the *Au/Graphene/p-Si/Al* sample, the Ψ_s–V change at 320 K is shown in Fig. 10a, and the $\Psi_s - V$ changes at all temperatures in the 120–320 K range are shown in the inset of this figure. The Φ_b and n values calculated with the help of the $\Psi_s(I_c,V_c)$, V_c, and $1/n$ values determined from these graphs are presented in Table 1. At the same time, variations of n and Φ_b values obtained by this method depending on sample temperature are shown in Fig. 10b. It is seen that both parameters are strongly dependent on sample temperature. Again, the linear relationship between n and Φ_b is shown in the graph in the inset of this figure. From this linear relationship, Φ_b = 0.820 eV was obtained for n = 1. As stated earlier, the n–Φ_b–T relationship can be explained by the lateral inhomogeneities of the potential barrier height.

Cibils and Buitrago have revised the Norde function as follows [52]:

$$F(V) = V - V_a \ln(I) \tag{9}$$

where V_a is a voltage parameter. In this method, the current values (I_0) corresponding to the minimum of the $F(V)$ function are determined by drawing $F(V)$–I plots for different values of V_a by using the forward bias current and voltage values. The relationship between I_0 and V_a is defined as follows:

$$I_0 = \frac{V_a}{R_s} - \frac{nkT}{qR_s} \tag{10}$$

Taking advantage of this linear relationship between I_0 and V_a, the values of n and R_s can be recalculated. Cibils curves derived as a function of V_a for the *Au/Graphene/p-Si/Al* structure are shown in Fig. 11a for T = 320 K and in Fig. 11b for T = 120 K, respectively. The linear relationship between I_0 and V_a is given in the inset of this figures. With the help of Eq. 10, n and R_s values were determined by using I_0–V_a linear relations prepared in the 120–320 K temperature range and these values are presented in Table 1. It is seen that the ideality factor values obtained from the Cibils function are in accordance with the values obtained from the I–V method. However, it is seen that the series resistance values obtained from the Cibils method are quite high when compared with the Norde method. This difference may be due to the fact that the Cibils method is very sensitive to voltage steps. The variation of the n and R_s values obtained from the Cibils method depending on the sample temperature is shown in Fig. 11c. It is clearly seen from these plots that both n and R_s values decrease linearly with increasing sample temperature. As stated earlier, the strong temperature dependence of the n and R_s values may be due to the inhomogeneity of the potential barrier height and lack of free carrier concentration at low temperatures, respectively.

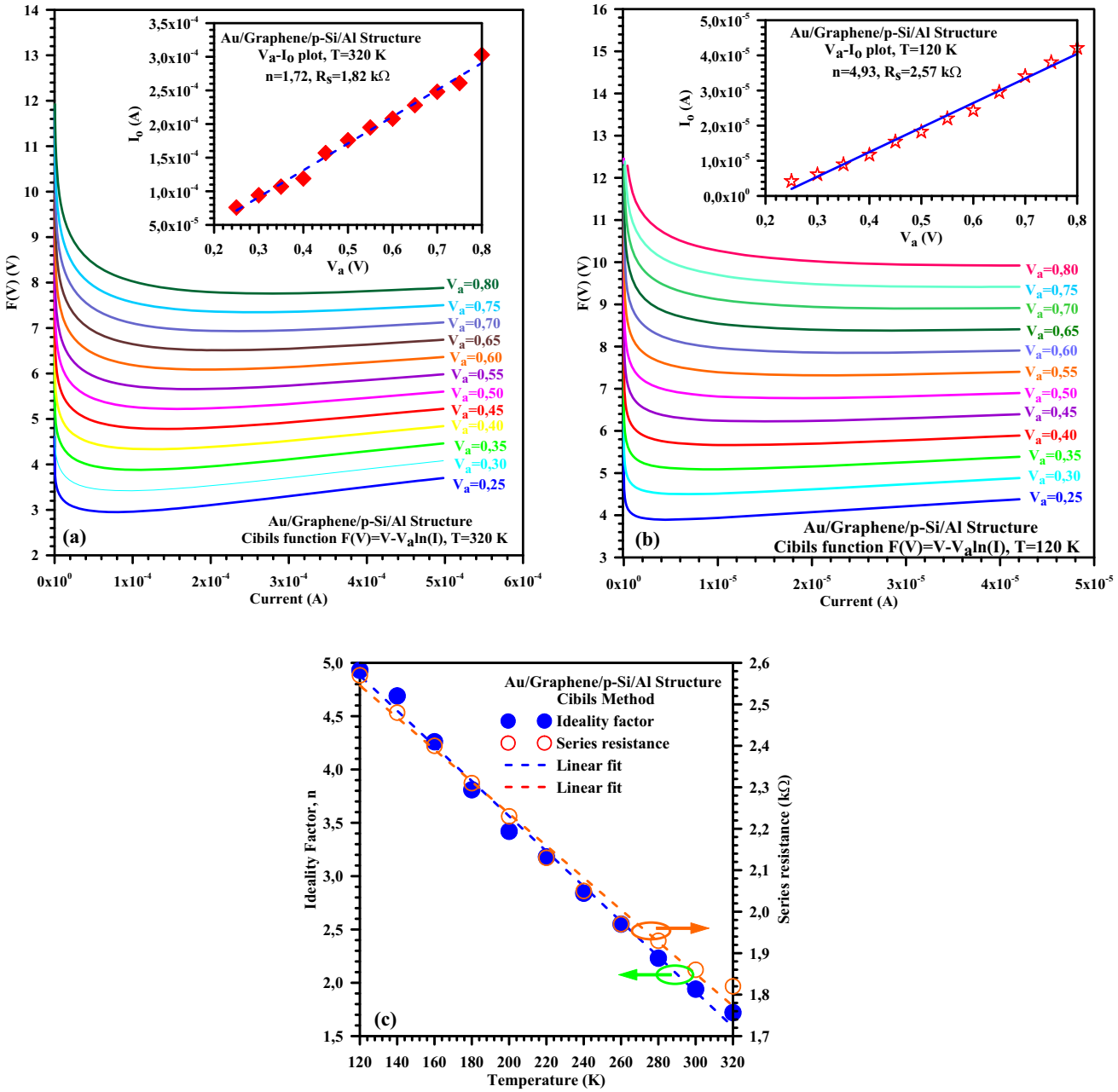


Fig. 11 Experimental plots obtained with the help of Cibils function $F(V)$. $F(V)$–I plots for different V_a values **a** at T = 320 K and **b** at 120 K. The I_0–V_a relationships are shown in the inset of this figures. **c** Variations of n and R_s obtained from the Cibils model depending on the sample temperature

Considering the n and R_s values obtained from the Norde and Cibils methods, corrections were made in the experimental forward bias ln(I)–V and I–V characteristics. The theoretical, experimental, corrected Norde, and corrected Cibils forward bias ln(I)–V characteristics at T = 300 K are shown in Fig. 12 and I–V characteristics are also shown in the inset of this figure. It is clear from this figure that the downward bending of the experimental plot due to the series resistance effect is significantly corrected by both the Norde and Cibils methods. That is, it can be said that the experimental forward bias I–V curve approximates significantly to the theoretical (ideal) curve with the corrections made with the help of Norde and Cibils methods. In this analysis, with the help of the parameters n and R_s obtained from Norde and Cibils

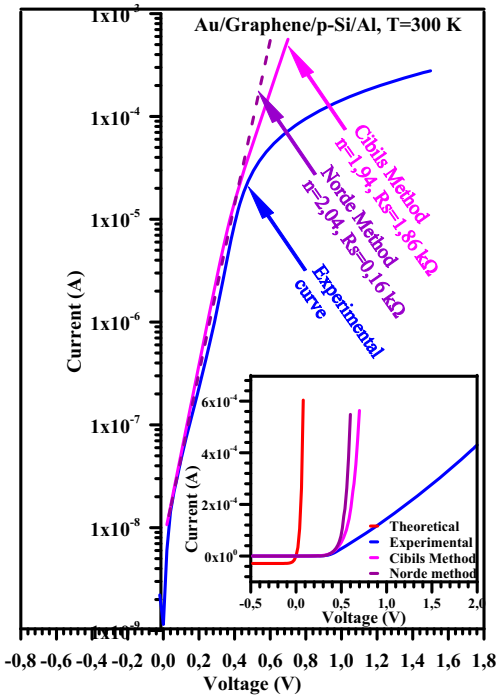


Fig. 12 Experimental, corrected Norde and corrected Cibils forward bias ln(*I*)–*V* curves for the *Au/Graphene/p-Si/Al* structure at T = 300 K. The forward bias *I*–*V* curves are also shown in the inset of this figure

methods, *I*–*V* characteristics were remodeled and it was seen that the curves obtained with these models were in good agreement with the experimental curve at low voltages. However, the modeled *I*–*V* characteristics differ from the experimental data at high voltages. This situation can be interpreted as showing the accuracy of the calculated diode parameters.

The inhomogeneous barrier model presents that the apparent barrier height value is smaller than the average value of the barrier height with the following relation [53]:

$$\Phi_{ap} = \Phi_{bo} - \frac{q\sigma_s^2}{2kT} \tag{11}$$

where Φ_{ap} is the apparent barrier height, $\Phi_{bo}i$ s the mean barrier height, and σ_s is the standard deviation of the barrier height. Again, according to this model, the relationship between apparent ideality factor (n_{ap}) and temperature is as follows:

$$\frac{1}{n_{ap}} - 1 = -\rho_2 - \frac{q\rho_3}{2kT} \tag{12}$$

where ρ_2 and ρ_3 are the voltage coefficients of the mean barrier height and the standard deviation, respectively. Considering Eqs. 11 and 12, Φ_{ap}—$1/2kT$

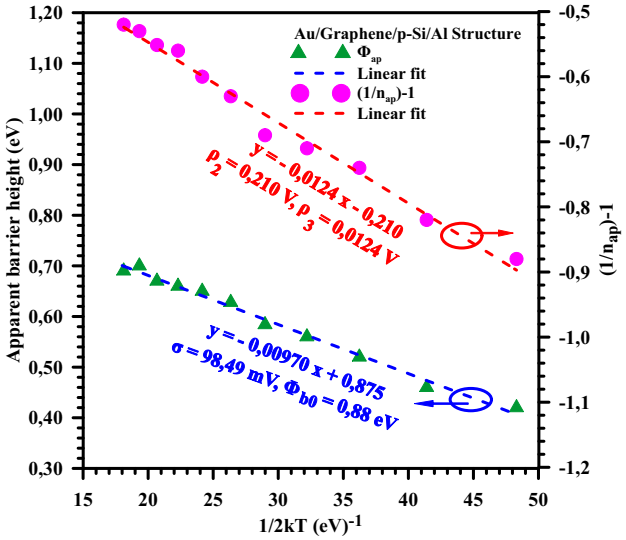


Fig. 13 The Φ_{ap} versus $1/2kT$ and $n^{-1} - 1$ versus $1/2kT$ plots for the *Au/Graphene/p-Si/Al* structure according to the Gaussian distributions of the barrier height

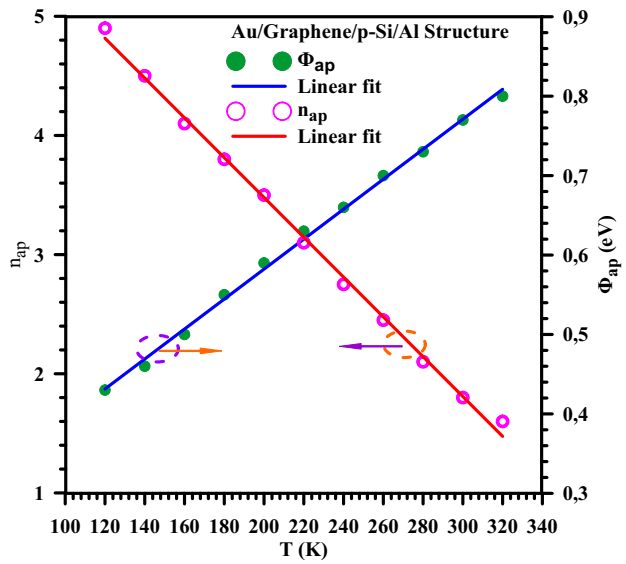


Fig. 14 The Φ_{ap} versus T and n_{ap} versus T plots for the *Au/Graphene/p-Si/Al* structure

and $((1/n_{ap}) - 1)$—$1/2kT$ plots were drawn and presented in Fig. 13. Φ_{bo} was calculated as 0.880 eV from the intersection of the Φ_{ap}—$1/2kT$ plot and σ_s was calculated as 98.49 mV from its slope. Similarly, ρ_2 was calculated as 210 mV from the intersection of the $((1/n) - 1)$—$1/2kT$ plot and ρ_3 was calculated as 12.4 mV from its slope. Also, the dependence of Φ_{ap} and n_{ap} on temperature is shown in Fig. 14. This graph shows that, as expected, Φ_{ap} increases linearly

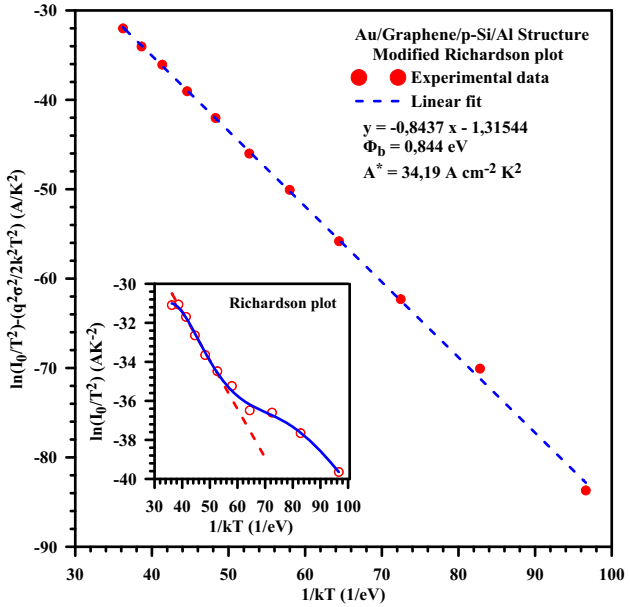


Fig. 15 Modified Richardson $\ln(I_0/T^2) - q^2\sigma_s{}^2/2k^2T^2$ versus $1/T$ plots for the *Au/Au-RGO/p-Si/Al* structure. Richardson $\ln(I_0/AT^2)$ versus $1/T$ plot is also shown in the inset of this figure

with temperature and n_{ap} also decreases linearly with temperature.

With the help of Eq. 2 arranged as follows, Richardson constant and barrier height values can be calculated:

$$\ln\left(\frac{I_o}{AT^2}\right) = \ln A^* - \frac{q\Phi_b}{kT} \tag{13}$$

According to this equation, the $\ln(I_o/AT^2)$ versus $1/kT$ plot should change linearly, and the Richardson constant can be calculated from its intersection, and the barrier height value from its slope, respectively. However, it appears that the $\ln(I_o/AT^2)$ versus $1/kT$ variation given in the inset of Fig. 15 is non-linear and therefore A^* and Φ_{bo} could not be calculated from this graph. It deviated significantly from linearity especially at low temperatures. This abnormal behavior is due to the shape of the potential barrier in the junction [48]. In non-homogeneous barrier-height diodes, the potential barrier located in the junction area consists of patches of different heights, and in this case, it causes the $\ln(I_o/AT^2)$ versus $1/kT$ plot to deviate from linearity. In such cases, a modified Richardson plot must be drawn to obtain correct values for the Richardson constant and the barrier height.

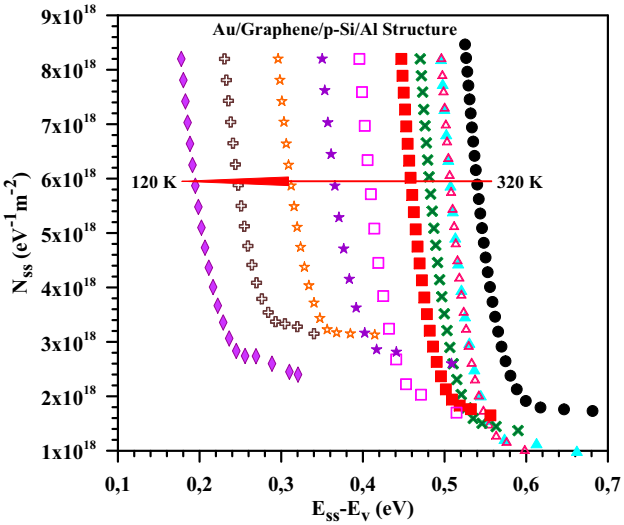


Fig. 16 The *Nss–(Ess–Ev)* plots of the *Au/Graphene/p-Si/Al* structure as a function of the sample temperature

By combining Eqs. 2 and 11, the modified Richardson equation can be arranged as follows:

$$\ln\left(\frac{I_o}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln AA^* - \frac{q\Phi_{bo}}{2kT} \tag{14}$$

According to this equation, the graph $\ln\left(\frac{I_o}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right)$ versus $1/kT$ should change linearly and the slope should give the value of the mean barrier height and the intersection (= $\ln AA^*$) should give the value of the Richardson constant (A^*). For the *Au/Graphene/p-Si/Al* structure, modified Richardson $\ln(I_o/T^2) - q^2\sigma_s^2/2k^2T^2$ versus $1/2kT$ plot drawn using Eq. 14 is given in Fig. 15. This graph has a straight line character over the entire temperature range of 120–320 K. The mean barrier height value from the slope of this straight line was obtained as 0.844 eV, and the experimental value of Richardson constant from the its intercept was obtained as 34.19 $Acm^{-2}K^2$. Therefore, it is seen that the mean barrier height value of 0.844 eV obtained from this plot is close to the value of 0.880 eV obtained from the Φ_{ap} versus $1/kT$ plot. Similarly, the 34.19 $Acm^{-2}K^2$ value obtained from this plot for Richardson constant is quite close to the theoretically calculated 32 $Acm^{-2}K^2$ value for *p-Si*. These results show that the values obtained from the modified Richardson plot by considering the Gaussian distributions of the barrier height are more reasonable for the *Au/Graphene/p-Si/Al* structure.

In such junctions, it is known that there is interface states (*Nss*) with different energies within the bandgap of the semiconductor during the production processes. These interfacial states are one of the major causes of downward concave curvature of the forward bias ln(*I*)–*V* characteristics at sufficiently large voltages. In this region, the ideality factor varies greatly depending on the size of the interfacial states. Therefore, the density of the interface states can be calculated from the data of the forward bias ln(*I*)–*V* characteristics in this region depending on the energy [54]. The *Nss* curves calculated by considering the dependence of both the ideality factor and the barrier height on the applied voltage are presented in Fig. 16 as a function of the sample temperature. It is clearly seen from Fig. 16 that the interface state density *Nss* has an exponential increase with the applied voltage from the top of the valence band to the mid-bandgap for each temperature and shifts toward the middle of the band with increasing sample temperature. Variations of the interface state density depending on the sample temperature can be interpreted by the thermal restructuring and rearrangement of the interface surface and the defect levels at the interface. When the current component created by some electrons captured by these interface states is added to the current component predicted by thermionic emission theory, the *I*–*V* characteristics of the diode are affected [55].

4 Conclusions

To fabricate the interface-layered *Au/Graphene/p-Si/Al* structure, first graphene thin film was grown on copper foil by PECVD method and then transferred to the clean and polished surface of the *p-Si* semiconductor base material. The characterization of the deposited graphene film was performed by SEM, AFM, XPS, and Raman spectroscopy methods. In order to examine the nature of the potential barrier formed at the *graphene/p-Si* interface of this structure fabricated under laboratory conditions and its effects on *I*–*V* characteristics, the forward and reverse bias *I*–*V* characteristics were measured in the temperature range of 120–320 K. Various characteristic parameters such as ideality factor, barrier height, saturation current, threshold voltage, rectification ratio, and series resistance, which give important clues about the functioning mechanism of this structure, were calculated from *I*–*V* measurements depending on the sample temperature using Rhoderick, Norde, Cibils, and Chattopadhyay methods. It has been observed that all of these characteristic parameters are strongly dependent on the sample temperature. The results were interpreted with the inhomogeneous barrier model using the Gaussian distributions of the mean barrier height. The mean barrier height value from the modified Richardson plot was calculated as 0.844 eV. In conclusion, inspired by the good rectification behavior of the *Au/Graphene/p-Si/Al* diode structure, we can say that graphene thin films produced by the PECVD method can be safely used as an interfacial layer in metal–semiconductor rectifier contacts.

Acknowledgements

This research was supported by the Ataturk University Scientific Research Management Office, under Project number: PRJ2016/160. The authors would like to thank Ataturk University Scientific Research Management Office for their support.

Author contributions

O.Ö. and B.G. contributed to conceptualization, visualization, investigation, and methodology. M.S. contributed to conceptualization, visualization, investigation, methodology, and writing-review & editing.

Funding

The authors did not receive support from any organization for the submitted work. The authors have no financial or proprietary interests in any material discussed in this article.

Data availability

The authors confirm that the data supporting the findings of this study are available within the article.

Declarations

Competing interest The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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